gem5 Workshop ISCA 2023

Validating Hardware and SimPoints with gem5:

A RISC-V Board Case Study

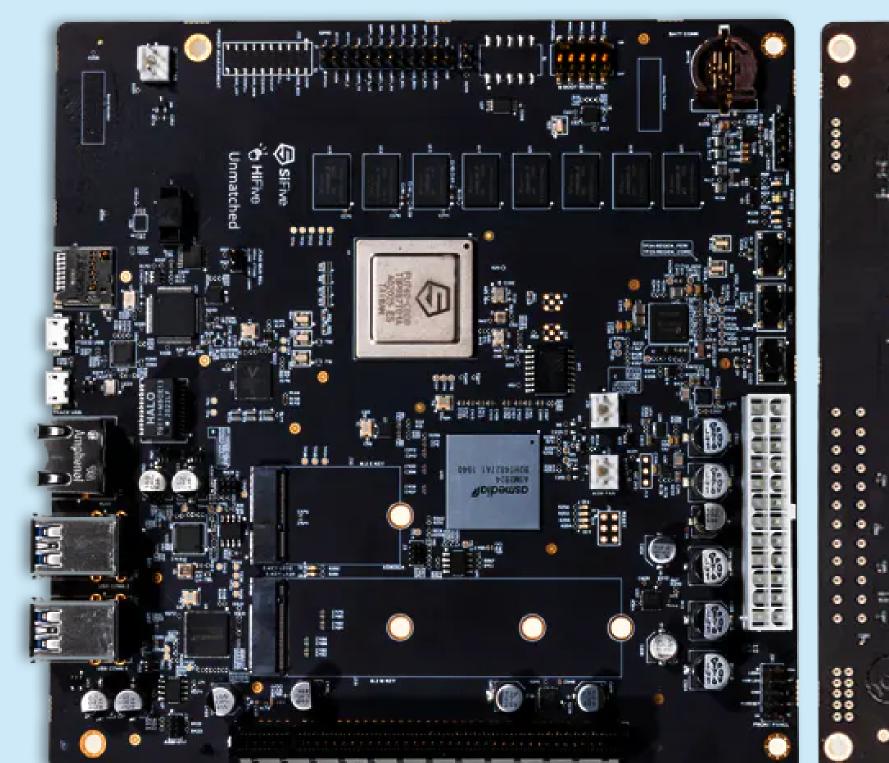
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ntroduction

- The RISCVMatched board is a **prebuilt** board in gem5, modeled after the SiFive Unmatched.
- Initializes all components (caches, core, memory, and processor).



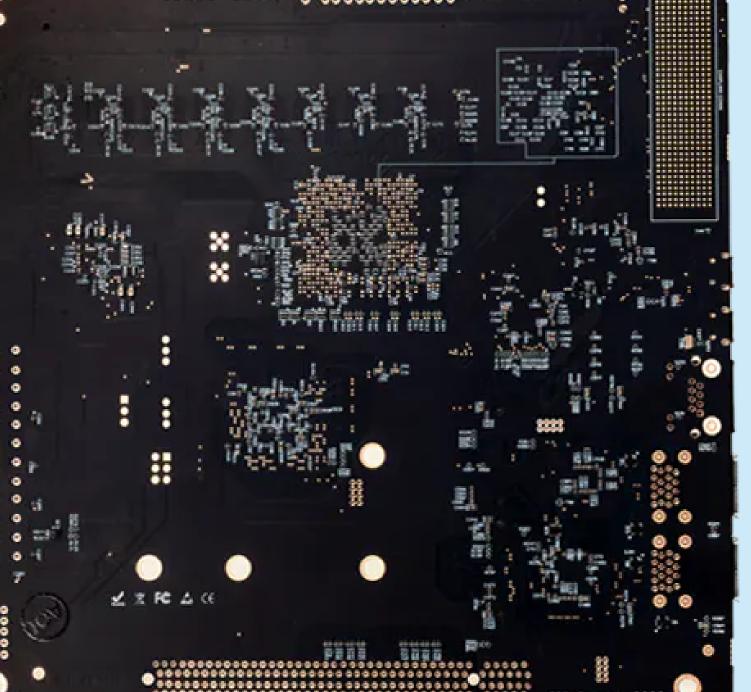


Fig. 1: The HiFive Unmatched by SiFive Inc.

Why SimPoints?

- **REQUIREMENT:** quick and reliable method to finetune configurations in gem5.
- By simulating and weighing program phases,
 SimPoints test successful configuration changes
 without running the benchmark to completion.

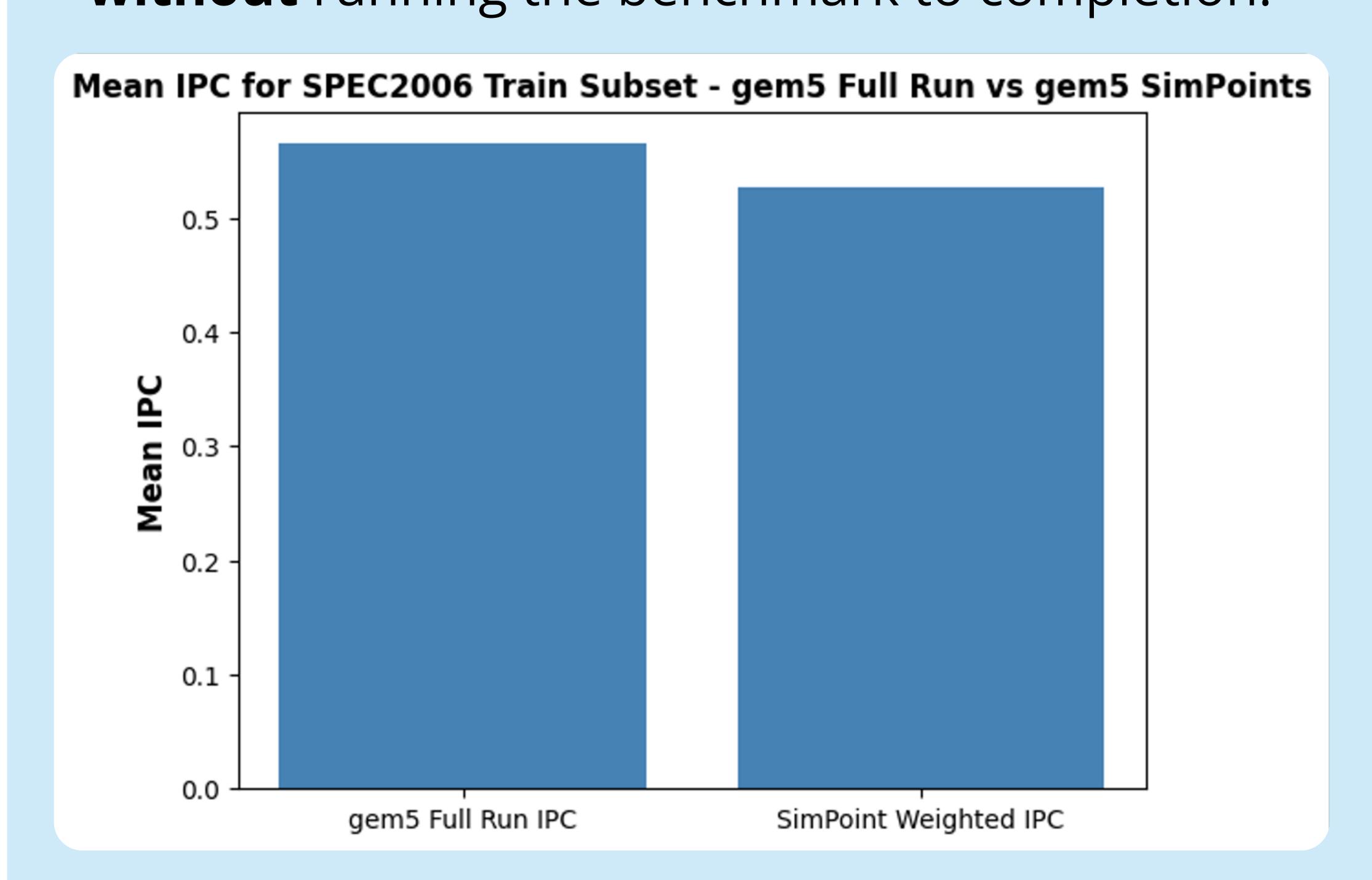


Fig. 2: Mean IPC for the SPEC2006 Subset – Train for a full run of gem5 and the mean weighted IPC of restoring the SimPoints for the workloads for the same configuration.

 Thus, weighted IPC from SimPoints is a good substitute for gem5 full runs.

DAVIS ARCHITECTURE RESEARCH



Methodology

- WORKLOADS: Microbenchmark Suite, found at https://github.com/VerticalResearchGroup/microbench
- IPC from hardware using perf; IPC from RISCVMatched in gem5; IPC ratio between gem5 and perf.
- Fine-tune the configuration for Mean Squared Logarithmic Error.
- Ran the new configuration on a **subset** of **SPEC2006** (all benchmarks that could complete full runs on gem5).
- · FINDING: Iterative microbenchmark fine-tuning, optimizing for IPC, systematically refines the configuration for larger workloads.

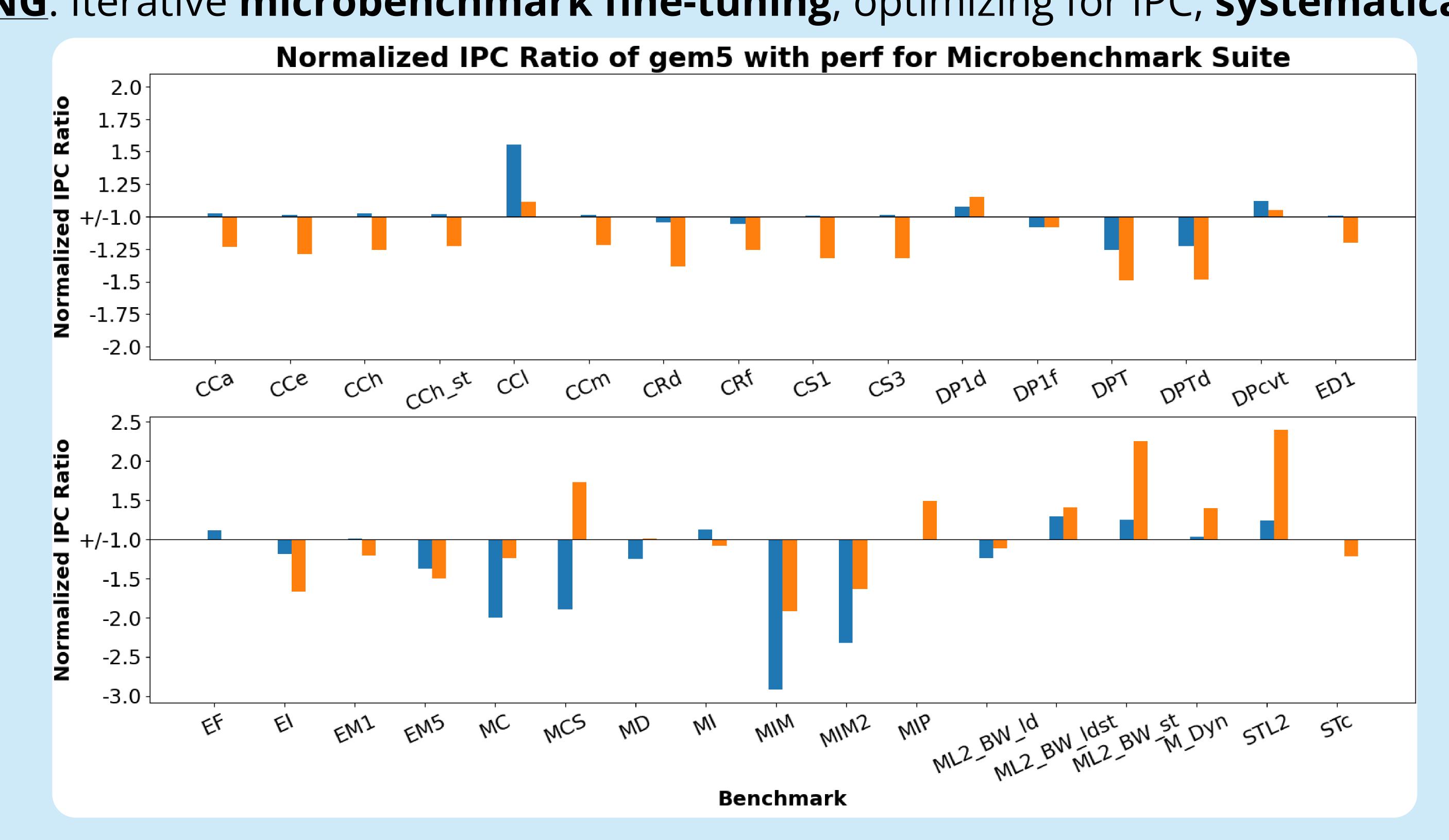


Fig. 3. Normalized IPC ratios of the edited configuration of the RISCVMatched (in blue) and the original configuration of the RISCVMatched (in orange) with respect to the perf baseline (+/-1.0).

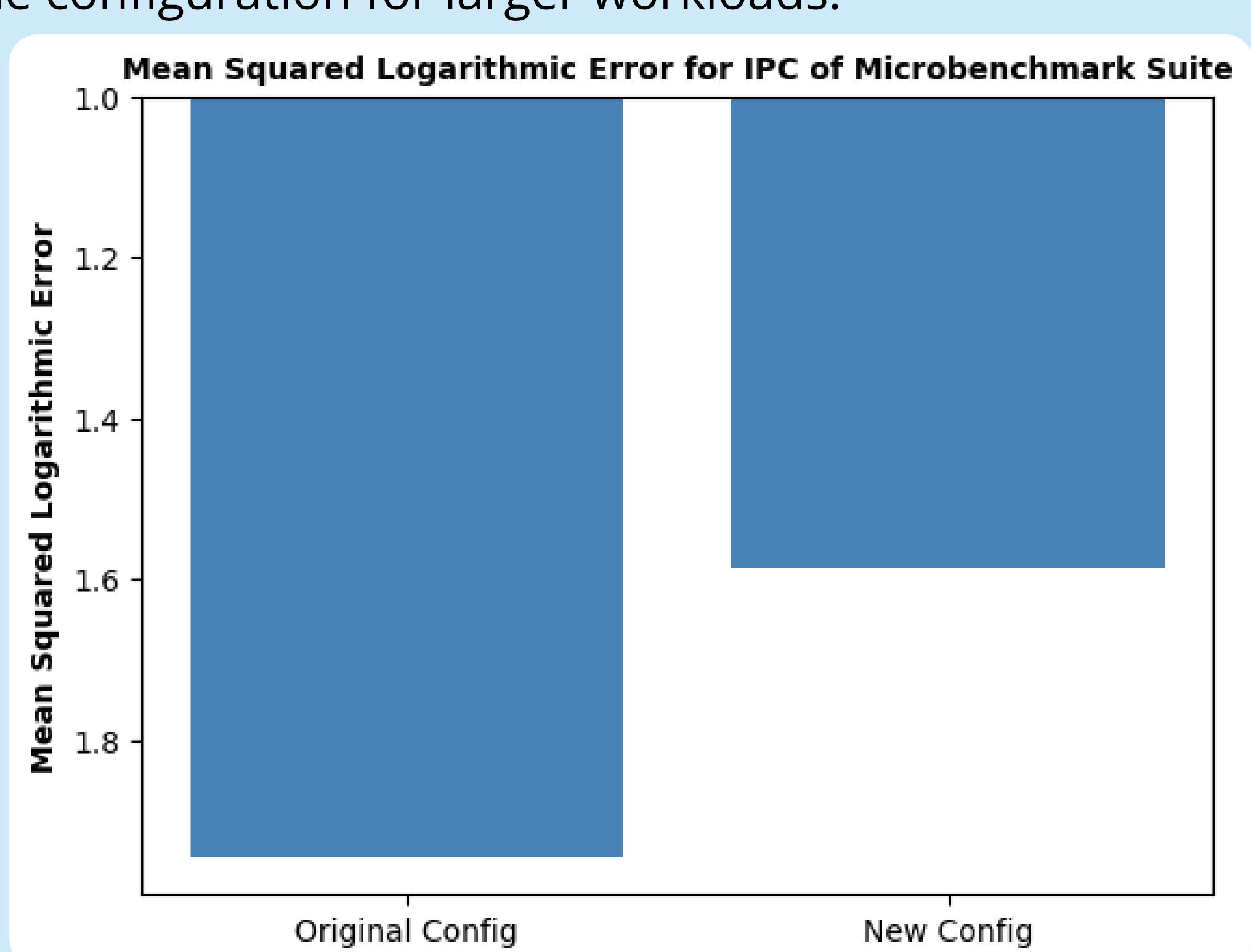
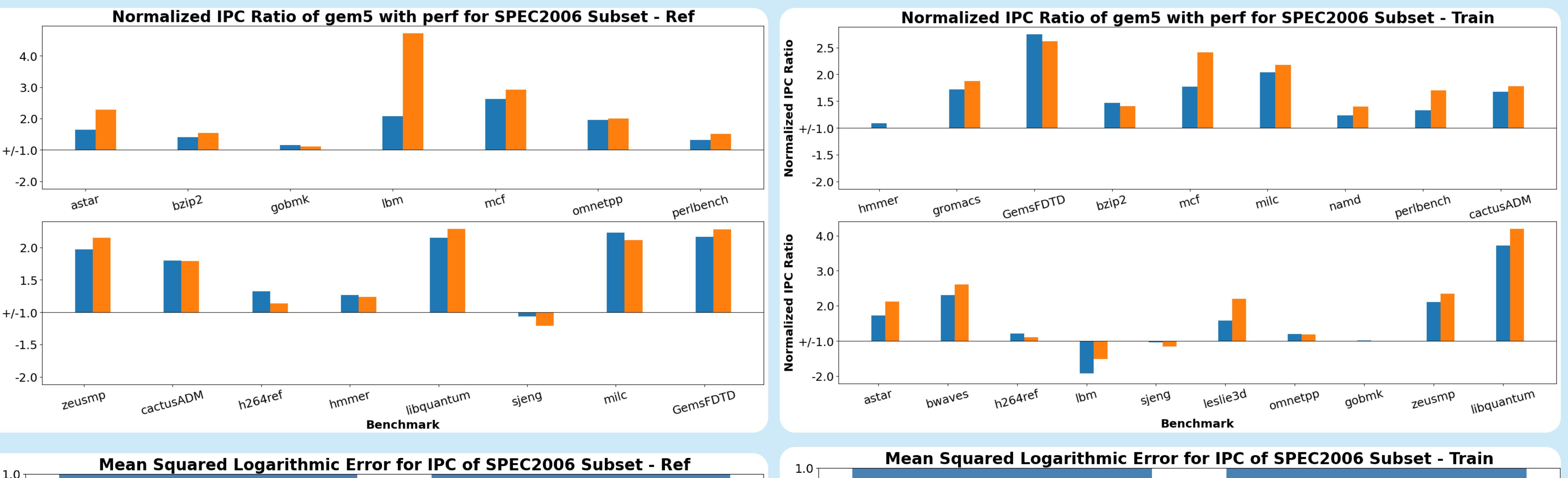
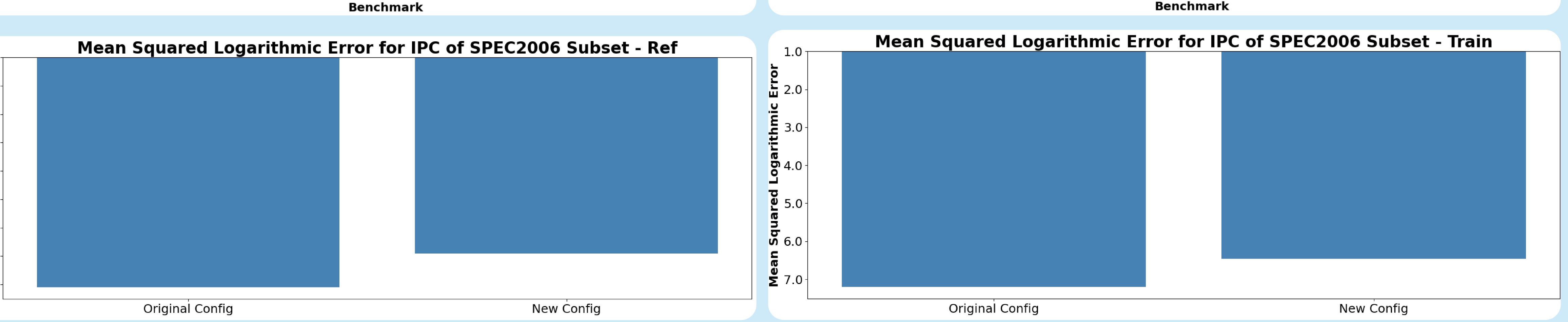


Fig. 4. Mean Squared Logarithmic Error for the IPC Ratio of the Microbenchmark Suite for the RISCVMatched's original configuration and the edited configuration.

SPEC2006 Results





Next Steps

- Make iterative microbenchmark fine-tuning automated.
- Extend methodology to OOO processors, LoopPoints and different ISAs.

References

[1] Jason Lowe-Power et al. 2020. The gem5 simulator: Version 20.0+. arXivpreprint arXiv:2007.03152 (2020). [2] T. Sherwood, E. Perelman, G. Hamerly, S. Sair and B. Calder, "Discovering and exploiting program phases," in IEEE Micro, vol. 23, no. 6, pp. 84-93, Nov.-Dec. 2003, doi: 10.1109/MM.2003.1261391. [3] T. Nowatzki, J. Menon, C. -H. Ho and K. Sankaralingam, "Architectural Simulators Considered Harmful," in IEEE Micro, vol. 35, no. 6, pp. 4-12, Nov.-Dec. 2015, doi: 10.1109/MM.2015.74. [4] S. Inc., SiFive FU740-C000 Manual v1p6, https://sifive.cdn.prismic.io/sifive/1a82e600-1f93-4f41-b2d8-86ed8b16acba_fu740-c000-manual-v1p6.pdf.

