



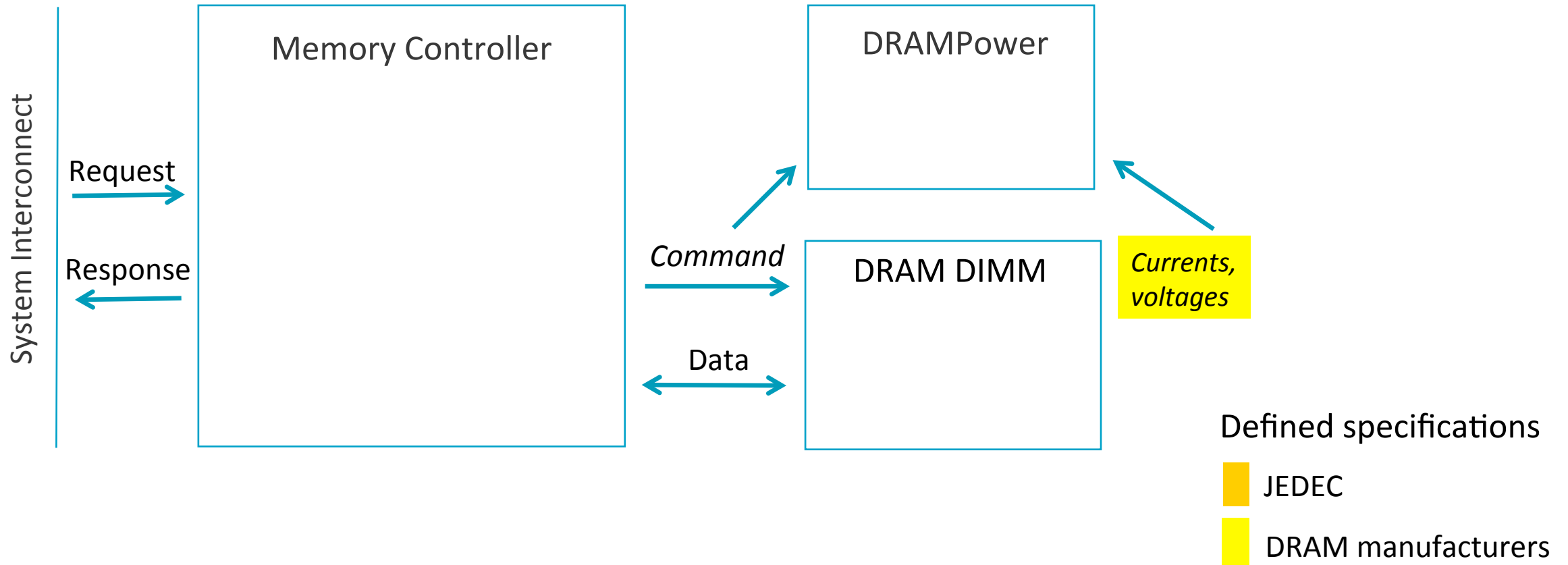
# DRAM Power-Down States in gem5

gem5 workshop at Arm Research Summit

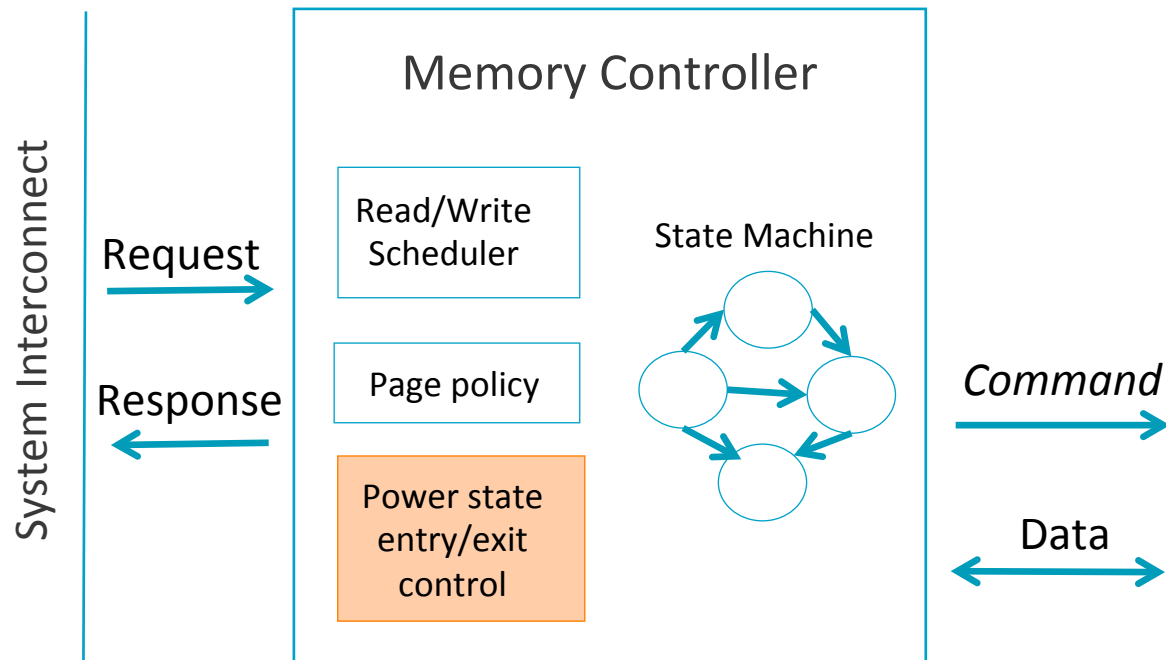
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# Background - DRAM in gem5



# Memory controller function



Reference for gem5 DRAM controller:  
A. Hansson, N. Agarwal, A. Kolli, T. Wenisch, and A.N. Udipi, *Simulating DRAM controllers for future system architecture exploration*, ISPASS 2014

## JEDEC defined states

- Active
- Idle
- Active Power-Down
- Precharge Power-Down
- Self-Refresh

Code committed, paper in MEMSYS Conference '17

Controller designers implement their own power state entry and exit control

# Scheduling power-down (PD) state transitions

## Conditions to enter power-down state

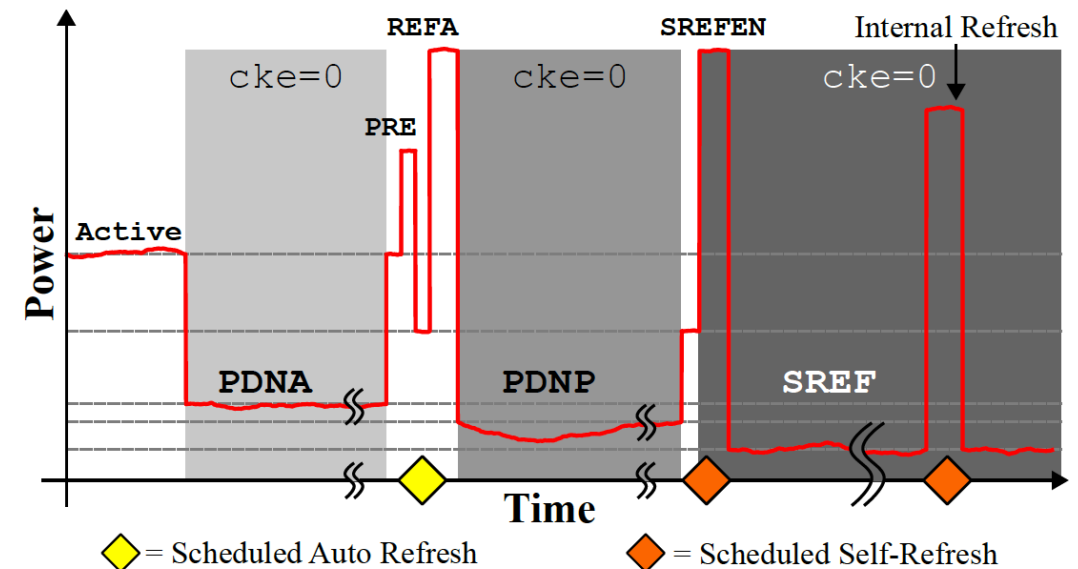
Enter power-down (PD) state if:

- There are no requests in the queue AND
- There are no pending events

Which PD state depends on:

- At least one bank open -> Active PD (PDNA)
- All banks closed -> Precharge PD (PDNP)
- Previous state was Precharge PD -> enter Self-Refresh (SREF)

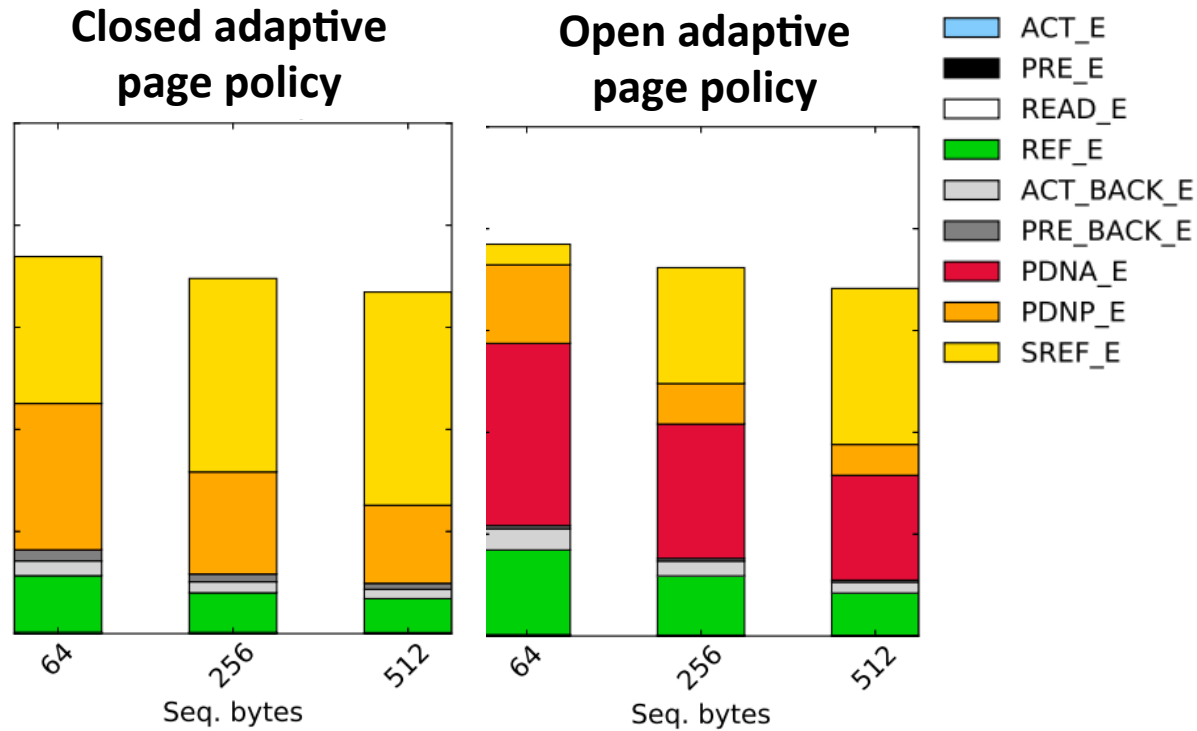
## Staggered power-down strategy



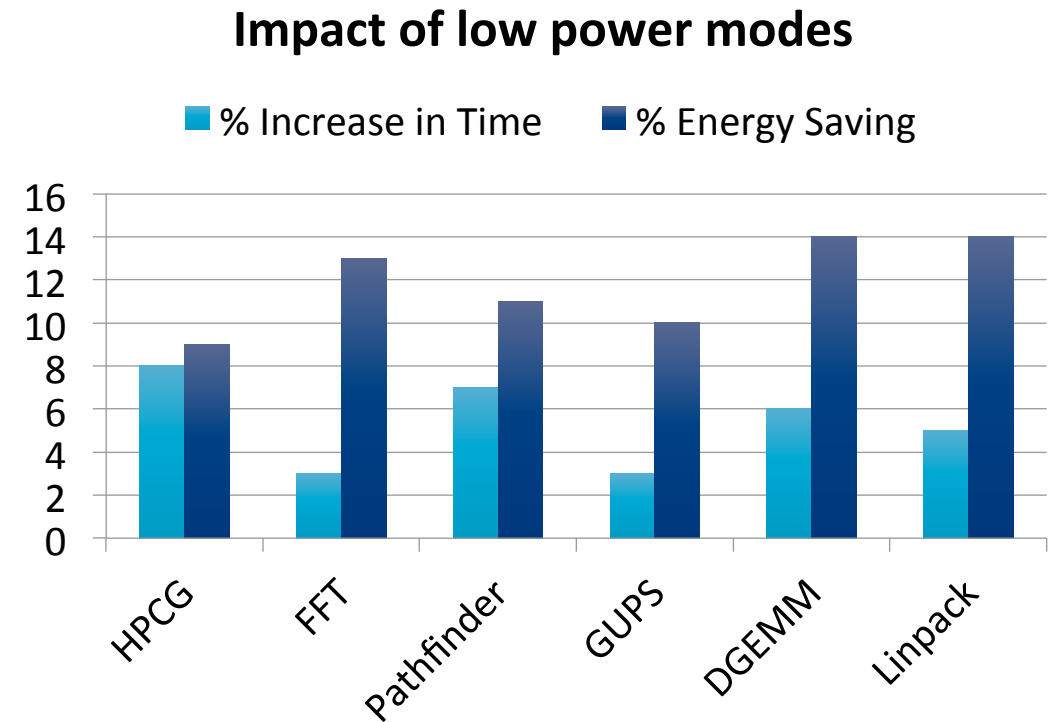
Reference: M. Jung, C. Weis, N. Wehn, M. Sadri, and L. Benini. 2014. Optimized active and power-down mode refresh control in 3D-DRAMs, VLSI-SoC 2014

# Do the PD modes work? What is their impact?

## Breakdown of energy per state



## Performance / energy trade-off



Memory part is based on 2 rank Micron DDR4-2400 8 Gbit datasheet

# Modeling details and validation results in MEMSYS '17 paper

DRAM is a major energy consumer and DRAM power-down modes are now integrated to enable richer full-system energy-efficiency studies

## Integrating DRAM Power-Down Modes in gem5 and Quantifying their Impact

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Thank You!

Danke!

Merci!

谢谢!

ありがとう!

Gracias!

Kiitos!

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